Digital Logic – ENGR 210 (3 credit hours)
Abilene Christian University
Fall 2015

Course Description
This course covers fundamental concepts of digital electronics, including unsigned, signed, and floating-point binary numbers, binary mathematical operations, error codes, Boolean algebra, Boolean logic simplification, Karnaugh maps, gate-level schematics, combinational logic, sequential logic, latches, flip-flops, counters, clocks, registers, and memory. Concurrent enrollment in Digital Logic Laboratory. Prerequisites: a grade of C or better in ENGR135/136 or PHYS 135/136.

Class Meeting Times and Location
This class meets Tuesday and Thursday in Foster Science Building Room 330 from 1:30 pm to 2:50 pm.

Required Text and Software
The required text for this course is *Digital Fundamentals,* by Thomas L. Floyd, 11th Edition, Prentice Hall, 2014, ISBN 978-0-13273-796-8.

Catalog Description
This course covers fundamental concepts of digital electronics, including binary numbers, binary mathematical operations, error codes, Boolean algebra, Boolean logic simplification, Karnaugh maps, gate-level schematics, combinational logic, sequential logic, latches, flip-flops, counters, clocks, registers, and memory. Prerequisites: a grade of C or better in ENGR135/136 or PHYS 135/136.

Contact Information
Name: Darby Hewitt, Ph.D., Assistant Professor of Engineering and Physics
Office: Foster Science 313-1
Phone: 325-674-2002
Email: darby.hewitt@acu.edu
Office Hours: MWF (10:00 am to 11:00 am) MT (3:00 pm to 5:00 pm). Additional office hours can be arranged as needed.

Teaching Philosophy
Engineering is a well-respected profession. The public entrusts engineers to be honest, competent, and ethical. Many codes of ethics for these fields indicate that the commitment to protecting the health, safety, and welfare of the public is of paramount importance. These values are in harmony with Christian principles and ideals. Christian engineers should be honest (Matthew 5:37), work hard to ensure competency (Colossians 3:23), and put the public's interest ahead of his or her own (Luke 6:31). In light of these principles, this course will be taught such that you will gain an appreciation for the professional nature of engineering. It will be taught so as to give you every opportunity to begin to develop competency in these fields. This will require homework, quizzes, tests, and group discussion. The instructor especially encourages the discussion of topics that would bear on integrating faith and professional responsibilities (cheating on licensure exams, weapons design and manufacture, environmental laws and employment opportunities in developing nations, etc.)

Learning Objectives and Course Competencies

ABET Learning Objectives	Course Competencies	Measurement
3(a) an ability to apply knowledge of mathematics, science, and engineering	Perform decimal to binary conversion and binary arithmetic with signed and unsigned binary numbers	Homework, Test 1, Final Exam
	Identify and interpret hexadecimal numbers in decimal format	Homework, Test 1, Final Exam
	Discuss error detection in transmitted binary information	Homework, Test 1, Final Exam
	Describe the functions of basic logic gates (NOT, AND, OR, NAND, NOR, XOR)	Homework, Test 1, Final Exam
	Analyze and simplify combinational logic circuits using Boolean algebra	Homework, Test 1, Final Exam
	Employ a Karnaugh map to simplify Boolean expressions	Homework, Test 1, Final Exam
	Explain the functions of adders, comparators, encoders/decoders, and multiplexers	Homework, Test 2, Final Exam
	Discuss the differences between latches and flip-flops	Test 2, Final Exam
	Relate the differences between registers and counters	Homework, Test 2, Final Exam
3(e) an ability to identify, formulate, and solve engineering problems	Design combinational logic circuits to perform functions expressed in Boolean algebra	Design Homework, Tests 1 and 2, Final Exam
	Construct basic latches using logic gates	Homework, Test 2, Final Exam

Student Conduct

Academic integrity is defined as academic work completed as assigned for each class by the individual or group responsible for the work. Violations of academic integrity and other forms of cheating involve the intention to deceive, mislead, or misrepresent and therefore, are a form of lying. Such actions are contrary to behavioral norms that flow from the nature of God. Academic misconduct includes, but is not limited to, the following: 1) Failure to give credit to sources used in a work in an attempt to present the work as one's own, 2) Submission of papers or projects obtained from another source (e.g., research service or club paper file) as one's own, and 3) Falsifying information orally or in writing. Academic misconduct may result in, but is not limited to, a zero on the assignment and/or an F in the course. Additionally, the department chair, Dean of the College of Arts and Sciences, and the Dean of Student Life will be notified. See the full university policy, including how to appeal a decision, by following this link:
http://www.acu.edu/campusoffices/studentlife/judicialDocuments/AcademicIntegrityPolicy.pdf.

Attendance

Attendance is expected at all class sessions. It is also expect that you arrive promptly. If you are absent or tardy it will negatively affect your participation, homework, quiz grades.

Grading Policy

Homework –

I encourage you to work together in small groups to solve homework problems, but ***do not copy your classmates' work.*** I expect homework to be turned in on time. It will typically be due a week after it is assigned, and will be assigned almost every week. ***No late homework will be accepted.*** If you simply cannot finish by the deadline, turn in what you have done on time to receive partial credit. I will drop your lowest homework grade.

Midterm Exams -

Two midterm exams will be given during the semester. The dates are tentatively shown in the schedule, but may be subject to change. You will have at least one week notice before tests. Make-up tests will only be given for university approved absences with my approval and **you must talk to me about it *before* the scheduled exam time.** Approved make-up tests will be given at an assigned time at my discretion. Make-up tests will be far more difficult than the in-class test and may be written or oral.

Final Exam -

The final exam will be given at the time scheduled by the university. It will be a cumulative survey of the material presented throughout the entire semester.

Calculation of Final Course Grade-

Homework.....33 %
Midterm Exams (2).....33 %
Final Exam.....34 %

90% and above . . . . . A

80% - 89% ..... B
70% - 79% C
60% - 69% ..... D
59% and below ..... F

ADA Compliance Statement

"Abilene Christian University is dedicated to removing barriers and opening access for students with disabilities in compliance with ADA and Section 504 of the Rehabilitation Act. The Alpha Scholars Program facilitates disability accommodations in cooperation with instructors. In order to receive accommodations, you must be registered with Alpha Scholars Program, and you must complete a specific request for each class in which you need accommodations. If you have a documented disability and wish to discuss academic accommodations, please call our office directly at 325-674-2667."

Disclaimer: This syllabus is complete and correct to my knowledge at the present time; however, this syllabus may be modified at any time if I determine that it is in the best interest of the class to do so.

The mission of the College of Arts and Sciences:
The College of Arts and Sciences engages students with humanity's greatest ideas to create understanding, apply insights, and serve the world as Christian thinkers and problem solvers.

The mission of ACU:
To educate students for Christian service and leadership throughout the world.

Digital Logic Course Schedule

Week, Day (excluding holidays)	Chapter(s)	Topics
1, T	2	(Syllabus overview), Binary numbers, Decimal to binary and binary to decimal conversion, (Homework 1 assigned)
1, R	2	Binary arithmetic, Signed binary numbers and arithmetic, Binary Coded Decimal (BCD)
2, T	2	Hexadecimal numbers, Floating point numbers, Digital codes, (Homework 1 due, Homework 2 assigned)
2, R	3	NOT (inverter), AND, OR, NAND, NOR, XOR, XNOR gates
3, T	3, 4	Defining gates in Verilog; Boolean operations and expressions (Homework 2 due, Homework 3 assigned)
3, R	4	Boolean laws and rules, DeMorgan's Theorems
4, T	4	Boolean analysis of logic circuits, simplification using Boolean algebra (Homework 3 due, Homework 4 assigned)
4, R	4	Standard forms of Boolean expressions; Boolean expressions and truth tables; Karnaugh maps
5, T	4	Karnaugh maps (continued), SOP simplification using Karnaugh maps, 5-variable Karnaugh maps, Quine-McCluskey method (Homework 4 due, Homework 5 assigned)
5, R	5	Basic combinational logic circuits, implementing combinational logic, combinational logic in Verilog
6, T	5	NAND/NOR logic, combinational logic using NAND/NOR gates

		(Homework 5 due, Homework 6 assigned)
6, R	5, 6	Logic circuit operation with pulse waveform inputs, Half adders
7, T	6	Full adders, parallel adders, ripple carry, look-ahead carry (Homework 6 due, Homework 7 assigned)
7, R	6	Comparators, Decoders, Encoders
8, T	6	Code conversion, multiplexers, demultiplexers, functions of combinational logic in Verilog (Homework 7 due, Homework 8 assigned)
8, R	6	Parity generation, parity checking; REVIEW for Test 1
9, T	2-6	TEST 1 (Homework 8 due)
9, R	7	Intro. to Sequential Logic, S-R Latch, gated S-R Latch, gated D Latch
10, T	7	Flip-Flops, Flip-Flop operating characteristics (Homework 9—design challenge assigned), flip-flops in Verilog
10, R	7	Applications of flip-flops, one-shots (monostable multivibrator), astable multivibrator
11, T	7	The 555 timer IC – a configurable multivibrator
11, R	8	Asynchronous and synchronous counters, up/down counters
12, T	8	Design of synchronous/asynchronous counters, cascaded counters (Homework 9 due, Homework 10—design challenge assigned)
12, R	8	Counter decoding, Applications of counters
13, T	8	Counters and their applications in Verilog
13, R	9	Types of shift registers, their applications, implementing shift registers in Verilog
14, T	7-9	TEST 2 (Homework 10 due, bonus Final Review assigned)
14, R	11	Programmable Logic Devices—FPGAs, CPLDs, SPLDs; Xilinx tool chain overview
15, T	11	Practical considerations for design implementation using FPGAs
15, R		Review for Final (bonus Final Review due)